ICU_P4032

The ICU_P4032 module contains the machine-dependent interrupt control unit code for the MIPS based Algorithmics P4032 evaluation board.

Target File Definitions

The values required in the target file depend on the model of CPU on the board.

ICU_IREGS	The memory location of the *interrupt request register* (IRR, read) and the *interrupt mask register* (IMR, write).
ICU_EREGS	The location of the *Panic interrupt request register* (IRR, read) and the *interrupt clear register* (ICR, write).
ICU_PREGS	The base of the PCI *interrupt request register* (PCI IRR, read), the PCI *interrupt mask register* (PCI IMR, write).

Shared Library Macros and Routines

icu_disable_interrupt

void *icu_disable_interrupt*(
uint *where*)

The *icu_disable_interrupt* routine masks out the interrupt with the vector *where* so that it will not generate a machine interrupt.

icu_enable_interrupt

void *icu_enable_interrupt*(
uint *where*)

The *icu_enable_interrupt* routine allows the device(s) associated with the interrupt vector *where* to generate a machine interrupt.

icu_add_handler

(void) *icu_add_handler*(
int *where*,
void (**rtn***)(int)**)

The *rome_add_handler* routine adds the routine *rtn* as a handler for the interrupt specified by the vector *where*.

icu_start_dma

(void) *icu_start_dma*(
void (**rtn***) (int)**)

icu_end_dma

(void) *icu_end_dma*(**void**)

icu_bus_error

(void) *icu_bus_error*(
int cause)